REMARKS

Claims 10-20 are pending in this application, with Claims 1-9 cancelled without prejudice to the filing of a divisional application, and Claims 10, 19 and 20 amended. The Applicant respectfully requests reconsideration and review of the application in view of the amendments and the following remarks. By the foregoing amendments, no new matter has been added.

The Applicant acknowledges with appreciation the indication of allowable subject matter in Claims 19 and 20. Per the Examiner's suggestion, the Applicant has redrafted Claims 19 and 20 to independent form. These claims are now considered allowable.

The Applicant further acknowledges that the Examiner has objected to Claim 10 for including certain informalities (i.e., missing punctuation). Accordingly, the Applicant has amended Claim 10 to correct the identified informalities.

Before addressing the merits of the rejections based on prior art, a brief description of the present invention is provided. Computer data is commonly stored in a variety of memory devices -- e.g., RAM, ROM, etc. While these devices differ in certain respects (e.g., RAM is capable of reading and writing data, ROM is only capable of reading data, etc.), they are typically constructed using similar technology. That is, most memory devices are divided into a plurality of addressable memory locations (i.e., each memory location has its own discrete address). This allows data to be stored in and/or retrieved from discrete memory locations having discrete memory addresses. While this has proven to be an effective way to manage (i.e., store and/or retrieve) large amounts of data, it may not be the most effective way to retrieve small amounts of read-only data. In other words, the time it takes to retrieve data from an address-based memory system may be excessive if only a small amount of data (in total) needs to be retrieved.

The present invention provides a system and method of minimizing read-only data retrieval time through the use of combinatorial logic (as oppose to retrieving read-

only data from discrete memory locations). Specifically, a binary-logic-function device is adapted to (i) receive a plurality of address bits, and (ii) utilize a plurality of logic functions (e.g., ORs, ANDs, XORs, NORs, etc.) to produce a plurality of binary values (i.e., read-only data values).

Depending on the number of address bits available, a number of logic functions can be defined through the use of combinatorial logic. For example, Figure 2 illustrates how combinatorial logic can be used to define sixteen logic functions (i.e., a-q) for two address bits (i.e., x, y). Specifically, function "a" is zero regardless of the value of each address bit, function "b" is one only when both address bits are one, etc. The results of each logic function are illustrated in Figure 3.

Once the functions are identified, they can be used to represent a plurality of read-only data values. For example, Figure 4 illustrates that the read-only data values of 4, 16, 20 and 32 can be represented by the function "ek ajaa" -- which represents the binary values of [(~x) & y], [~y], [0], [~(x ^ y)], [0], and [0], respectively, where "~" represents NOT, "&" represents AND, and "^" represents XOR. Thus, instead of using a relatively slow ROM to retrieve four read-only data values, a binary-logic-function device adapted to perform pre-determined logic functions is be used.

The Examiner rejected Claims 10-18 under 35 U.S.C. § 103(a) as being unpatentable over Leach et al. in view of Aipperspach et al. These rejections are respectfully traversed.

Leach et al. is directed toward a special-purpose microcomputer adapted to perform digital signal processing. As shown in Figure 1, the special-purpose microcomputer includes (i) a central processing unit (CPU) 12, (ii) a controller 14, (iii) a direct memory access (DMA) coprocessor 22, RAM devices 16, 18, (iv) a ROM device 20, peripheral ports 24-26, and memory ports 32a, 32d. See paragraphs 0083-84. A cursory review of the application, however, reveals that the ROM device depicted in Figure 1 is a standard prior-art ROM device (i.e., where each memory location has its own discrete address). See e.g., paragraph 0084, lines 9-13 ("Data bus 30 further

contains a first set of address lines 30a and a second set of address lines 30b, both of which are for communication of address signals corresponding to memory locations in memories 16, 18 and 20."); paragraph 0091, lines 10-12 ("Based on the output from address decoder 33, access is granted to the memory locations specified by the selected address signals); and paragraph 0092, lines 14-18 ("In the preferred embodiment, a single memory address space is provided for microcomputer 10, so that a given address signal presented on any given set of address lines of buses 30, 34 and 38 will address a memory location in only one of memories 16, 18 and 20.").

Aipperspach et al. is directed toward a system and method of generating/arranging macros for a VLSI (very large scale integrated) semiconductor circuit. Specifically, each macro is defined by a plurality of circuit blocks including (i) a control section, (ii) a bit decoder section, (iii) a word decoder section, (iv) a word selector section, (v) a bit selector section, and (vi) a sense latch driver section. See Figure 2 and col. 2, lines 48-57. Aipperspach discloses that the bit selector section (i.e., the bit decoder) may further include a plurality of logic function gates adapted to receive multiple inputs and provide multiple outputs. Col. 6, lines 5-18.

In making the aforementioned rejections, the Examiner characterized Leach as disclosing a read-only memory system in which read-only data is stored in combinatorial logic, citing paragraph 0150, lines 6-10 for support. The Applicant respectfully disagrees with such a characterization. First, the portion of Leach cited by the Examiner (i.e., paragraph 0150) is not directed toward a ROM device or even the computer's memory system, but instead the computer's controller 14 (as shown in Figures 1 and 7a). Specifically, paragraph 0150 identifies the controller's instruction register 94 and control logic 202, and describes how the control logic 202 uses combinatorial logic to decode instruction codes provided by the instruction register 94. Thus, while Leach discloses the use of combinatorial logic for the purpose of decoding instruction codes, it does not disclose the use of such a circuit to produce read-only data.

Second, while Leach discloses that a ROM or a programmable logic array can be used instead of combinatorial logic to decode the instruction codes, Leach does not disclose the use of combinatorial logic to operate as a ROM. The reason Leach discloses such a concept (i.e., using a ROM to decode instructions) is because a ROM, like combinatorial logic, operates to produce a particular result in response to a particular set of inputs. Thus, in certain circumstances, a ROM might be used instead of combinatorial logic to produce a particular result in response to certain inputs.

Netherless, this does not imply that a combinatorial logic circuit could be designed to replace a ROM (i.e., effectively the reverse situation). For example, the load constant instruction set for the Pentium processor includes seven read-only data values: (i) one, (ii) log base two of ten, (iii) log base two of e, (iv) pi, (v) log base ten of two, (vi) log base e of two, and (vii) zero. While these seven values could easily be stored in a ROM, it is not readily apparent that all seven of them could be represented by a single algorithm, or a combinatorial logic circuit. As the present application illustrates, the design of such a circuit requires identifying a plurality of logic functions (see e.g., Figure 2), defining particular arrangements of these logic functions to represent each and every one of the read-only data values (see e.g., Figures 5-6), and designing a circuit capable of carrying out the selected functions (see e.g., Figures 7-9). Not only does Leach fail to disclose such a process, but Leach only discloses the use of a prior art ROM (i.e., having discrete locations) to produce read-only data values. If it was known that combinatorial logic could be used to represent read-only data values, such a disclosure surely would have been made. Thus, it is clear that Leach fails to disclose this aspect of the present invention.

Furthermore, according to the Examiner, Aipperspach is cited merely for its disclosure of a logic function gate adapted to receive multiple inputs and produce multiple outputs. In other words, Aipperspach does not disclose (nor is it cited for its disclosure of) a ROM device or the use of combinatorial logic to represent the same. Thus, it is clear that neither Leach nor Aipperspach (either alone or in combination)

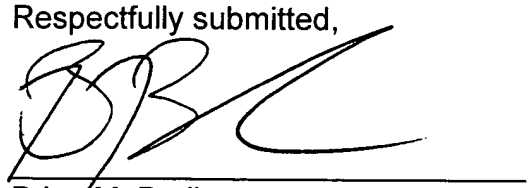
discloses or suggests the use of combinatorial logic to represent read-only data values.

More particularly, the Leach and Aipperspach references, either alone or in combination, fail to disclose or suggest a "read-only memory system where read-only data is stored in combinatorial logic, said system comprising: at least one binary logic function device adapted to receive two binary address bits and to generate a plurality of binary values from said two address bits and a plurality of logic functions, said read-only data including at least one of said plurality of binary values," as defined in Claim 10. Therefore, the rejection of independent Claim 10, as well as the rejections of Claims 11-18, which depend therefrom, should be withdrawn.

In view of the foregoing, the Applicant respectfully submits that Claims 10-20 are in condition for allowance. Reconsideration and withdrawal of the rejections is respectfully requested, and a timely Notice of Allowability is solicited. To the extent it would be helpful to placing this application in condition for allowance, the Applicant encourages the Examiner to contact the undersigned counsel and conduct a telephonic interview.

While the Applicant believes that no fees are due in connection with the filing of this paper, the Commissioner is authorized to charge any shortage in the fees, including extension of time fees, to Deposit Account No. 50-0639.

Respectfully submitted,



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